a switch circuit which includes second and third transistors controlled to turn on/off by said control circuit, each having a threshold voltage higher than that of each of said first transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line by simultaneously turning off said second and third transistors;

wherein said some gate circuits are provided on a critical path.

REMARKS

Favorable reconsideration of this application as presently amended in light of the following discussion is respectfully requested.

Claims 1 and 3-17 are presently active in this case. Claim 2 has been canceled and claim 1 has been amended by way of the present amendment.

In the outstanding office action, claims 1 and 2 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 6,288,586 to Ahn; claims 3 and 4 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,208,170 to Iwaki et al.; claims 8-10 rejected under 35 USC 102(e) as being anticipated by JP-6-29834; and claims 14 and 16 were rejected under 35 USC 103(a) as being unpatentable over Iwaki et al. in view of JP-6-29834. Claims 5-7, 11-13, 15, and 17 were indicated as being allowable.

First, applicants acknowledge with appreciation the indication that claims 5-7, 11-13, 15, and 17 were indicated as being allowable.

Briefly recapitulating, the present invention (Claim 1 as amended) provides that only the gate circuit on the critical path in the semiconductor integrated circuit is composed of a logic circuit formed of first transistors having a low threshold voltage and a switch circuit formed of second and third transistors having the high threshold voltage.

Because the logic circuit includes the first transistors having the low threshold voltage, it is possible to speed up the signal transmission on the critical path. The logic circuit including the first transistors having the low threshold voltage may increase the leak current. However, because the present invention cuts off the leak path with the switch circuit, it is possible to reduce the power consumption. Hence, claim 2 has a feature with which it is possible to speed up the signal transmission on the critical path and to reduce the power consumption.

In contradistinction thereto, Ahn connects the PMOS transistor and the NMOS transistor, which corresponds to the switch circuit of the present invention, to all the logic circuits regardless of whether they are on the critical path or not, thereby reducing the leak current in the standby state. Consequently, the sizes of the PMOS transistor and the NMOS transistor constituting the switch circuit have to be increased, or the number of the PMOS transistor and the NMOS transistor has to be increased. Accordingly, there is a problem in that the circuit size increases.

As defined by claim 1 of the present application, only the gate circuit on the critical path includes the logic circuit including the first transistors having the low threshold voltage. Thus, it is possible to reduce the area in which the switch circuit has to be provided, as compared with Ahn. Accordingly, it is possible to downsize the circuit to a larger degree, as compared with Ahn. Thus, it is not believed that Ahn anticipates the subject matter defined by claim 1.

Claims 3-4

Independent claim 3 defines that the gate circuit is connected between the virtual voltage line and the first reference voltage line, and that the second transistor is connected between the virtual voltage line and the second reference voltage line. Because the gate

circuit is directly connected to the first reference voltage line, if the second transistor is turned off, it is possible to surely cut off the leak path of the gate circuit.

In contradistinction thereto, as illustrated in the circuit of Fig. 4 of Iwaki, the gate circuit 301 and the transistor 105 are connected in series between the virtual voltage line QVCC and the ground line VSS. Because the gate circuit 301 of Iwaki is not directly connected to the ground line VSS, the leak current may flow through via the transistor 105. Consequently, Iwaki neither discloses nor suggests a configuration for directly connecting the gate circuit to the first reference voltage line and is thus not believed to anticipate the subject matter defined by claim 3.

Independent Claim 8 defines a storage circuit capable of holding output logic of the gate circuit. In contradistinction thereto, the high threshold logic circuit 30 of JP6-29834 does not hold the output logic of the low threshold logic circuit 20, but rather latches data inputted to the high threshold logic circuit 30 by the clock CK outputted from the low threshold logic circuit 20. Furthermore, as provided for by JP6-29834, the timing in which the high threshold logic circuit 30 holds data is prescribed by the logic of the clock signal CK inputted to the low threshold logic circuit 20. The timing does not depend on the ON/OFF status of the transistors TS1, TS2, TS5 and TS6 capable of cutting off the leak path of the low threshold logic circuit 20 and the high threshold logic circuit 30.

The storage circuit of claim 8 is configured such that the timing for performing the holding operation synchronizes with the timing in which the second and third transistors turn on/off. Such a circuit operation is neither discloses nor suggested by JP6-29834. Hence, JP6-29834 is not believed to anticipate the subject matter defined by claim 8.

In light of the above discussion, it is respectfully submitted that claims 1, 3, and 8 are patentably distinguishable from the applied patents, and the dependent claims thereof are therefore also patentably distinguishable from the applied patents.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,
OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

W. Todd Baker

Gregory J. Maier
Registration No. 25,599
Attorney of Record
W. Todd Baker
Registration No. 45,265

22850

Tel.: (703) 413-3000
Fax: (703) 413-2220
I:\atty\Wtb\210067US\210067US-AM2.wpd

Marked-Up Copy
Serial No: 09/883,959
Amendment Filed on: November 1, 2002

IN THE CLAIMS

--1. (Twice Amended) A semiconductor integrated circuit comprising:

a plurality of gate circuits; and

a control circuit configured to control the operation of some gate circuits among said plurality of gate circuits,

each of said some gate circuits among said plurality of gate circuits including:

a logic circuit constituted by a plurality of first transistors; and

a switch circuit which includes second and third transistors controlled to turn on/off by said control circuit, each having a threshold voltage higher than that of each of said first transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line by simultaneously turning off said second and third transistors;

wherein said some gate circuits are provided on a critical path.

2. (Canceled)--